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(54) Semiconductor memory device.

(57) A semiconductor memory device comprising a memory cell array having a plurality of dynamic memory cells (MCi), each of the memory cells including a plurality of MOS transistors (Q1 - Q4) connected by cascade connection, capacitors (C1 - C4) for storing data each having an end connected to an end of a corresponding one of the MOS transistors, and a register arranged in a column portion of the memory cell array, for temporarily registering the data read from the memory cells in a time series manner.

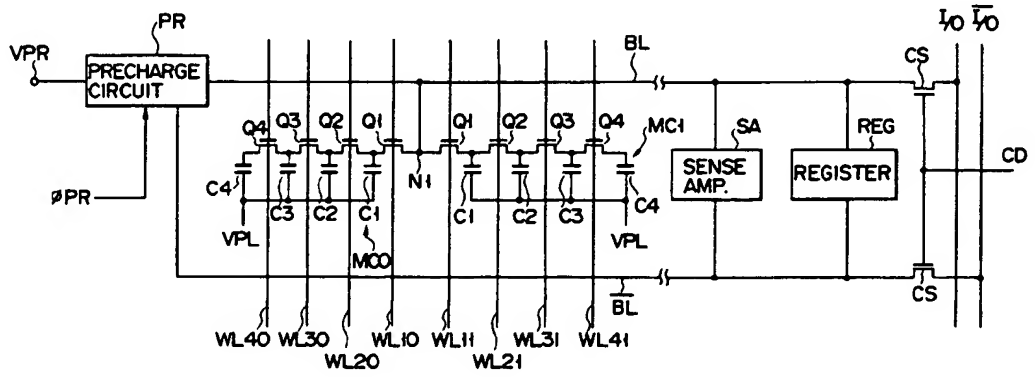


FIG. 3

This invention relates to a semiconductor memory device, and more particularly to a dynamic random access memory (DRAM).

Most DRAM cells put in practice in these days each comprise an (insulating gate type) MOS transistor serving as a transfer gate and connected to a word line and to a bit line, and a capacitor connected to the MOS transistor for storing data.

To more highly integrate DRAM cells to thereby reduce the cost of each bit, the inventor of the invention has proposed, in USA application serial No. 6 8 7, 6 8 7, cascade gate type semiconductor memory cells shown in Figs. 1 and 2.

The DRAM cell shown in Fig. 1 comprises MOS transistors Q1 - Q4 connected by cascade connection, and capacitors C1 - C4 each having one end connected to one end of the corresponding transistor Q1 - Q4, for storing data. By turning on and off the transistors Q1 - Q4 in a predetermined order, data items are successively read to a read-out/write-in node 1 which is connected to a bit line BL from the capacitors C1, C2, C3, and C4 in the order mentioned, i.e., in the order from the capacitor closest to the bit line BL to that remotest therefrom. Similarly, the read-out write-in data items are written from the node 1 into the capacitors C4, C3, C2, and C1 in the order mentioned, i.e., in the order of from the capacitor remotest from the bit line BL to that closest thereto.

The DRAM cell shown in Fig. 2 is similar to that shown in Fig. 1 except that it further incorporates a second node N2 and a MOS transistor Q5 connected between the transistor Q4 and the second node N2. Also in the DRAM cell of Fig. 2, by turning on and off the transistors Q1 - Q5 in a predetermined order, data items are successively read to the node 1 from the capacitors C1, C2, C3, and C4 in the order mentioned, and the read-out/write-in data items are written from the node 2 into the capacitors C1, C2, C3, and C4 in the order mentioned.

The above-described cascade gate type memory cells shown in Figs. 1 and 2 can store data of a plurality of bits in units of one bit. Thus, as compared with a conventional DRAM consisting of an array of cells each having a transistor and a capacitor, a remarkably highly integrated DRAM can be formed of an array of memory cells of the cascade gate type, thereby much reducing the cost of one cell or bit, since only one contact is required in the latter case to connect a plurality of cells or bits to a bit line.

In the DRAM made of cascade gate type memory cells, however, data stored in each cell is read out in a destructive read out manner, so that it is always needed to rewrite data into the cell. But, rewriting new data into any capacitor cannot be performed immediately after the stored data is read out, since in any memory cell of the cascade gate type, the order of the capacitors from which the stored data is read out is predetermined. That is, rewriting can be performed for the first time after data stored in all the capacitors are read out completely.

Thus, the DRAM comprising of a cascade gate type memory cell array must have means for rewriting (or writing) data in order into the capacitors employed in each cell, after data of a plurality of bits are read out of the cell.

This invention has been made in consideration of the above-described circumstances, and therefore has the object to provide a semiconductor memory device consisting of a high density and hence low-bit-cost DRAM including a cascade gate type memory cell array, in which a plurality of data items are read from a memory cell in a time series manner, and then successively be rewritten (or written) into the memory cell.

To attain the object, the memory device of the invention comprises a memory cell array having a plurality of dynamic memory cells, each of the memory cells including a plurality of MOS transistors connected by cascade connection, capacitors for storing data each having an end connected to an end of a corresponding one of the MOS transistors; and register means arranged in the column portion of the memory cell array, for temporarily registering the data read from the memory cells in a time series manner.

By virtue of the above structure, the semiconductor memory device of the invention can successively read data items from the capacitors of a memory cell to its bit line, then register them in register means, and successively write data items from the bit line into the capacitors.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a circuit diagram showing a cascade gate type memory cell which has been proposed;

Fig. 2 is a circuit diagram showing another cascade gate type memory cell which has also been proposed;

Fig. 3 is a circuit diagram showing a part of a DRAM of a first embodiment of the invention;

Fig. 4 is a circuit diagram showing an example of elements forming a register shown in Fig. 3;

Fig. 5 is a circuit diagram showing another example of elements forming the register shown in Fig. 3;

Fig. 6 is a circuit diagram showing a further example of elements forming the register shown in Fig. 3;

Fig. 7 is a circuit diagram showing an example

of elements shown in Fig. 6;
Fig. 8 is a circuit diagram showing another example of elements shown in Fig. 6;
Fig. 9 is a waveform timing chart illustrating the operation of the DRAM shown in Fig. 3;
Fig. 10 is a circuit diagram showing a part of a DRAM of a second embodiment of the invention;
Fig. 11 is a waveform timing chart illustrating the operation of the DRAM shown in Fig. 10;
Fig. 12 is a circuit diagram showing another register incorporated in the invention;
Fig. 13 is a circuit diagram showing a further register incorporated in the invention;
Fig. 14 is a waveform timing chart illustrating the operation of a DRAM according to a third embodiment of the invention;
Fig. 15 is a circuit diagram showing a part of a DRAM of a fourth embodiment of the invention;
Fig. 16 is a circuit diagram showing a part of a DRAM of a fifth embodiment of the invention;
Fig. 17 is a waveform timing chart showing the operation of the DRAM shown in Fig. 16;
Fig. 18 is a circuit diagram showing a part of a DRAM of a sixth embodiment of the invention;
Fig. 19 is a circuit diagram showing another example of elements forming a register shown in Fig. 18;
Fig. 20 is a diagram showing a circuit similar to that shown in Fig. 3, except that it incorporates a single end type sense amplifier in place of the sense amplifier shown in Fig. 3;
Fig. 21 is a diagram showing a circuit similar to that shown in Fig. 10, except that it incorporates a single end type sense amplifier;
Fig. 22 is a diagram showing a circuit similar to that shown in Fig. 15, except that it incorporates a single end type sense amplifier;
Fig. 23 is a diagram showing a circuit similar to that shown in Fig. 16, except that it incorporates a single end type sense amplifier; and
Fig. 24 is a diagram showing a circuit similar to that shown in Fig. 19, except that it incorporates a single end type sense amplifier.

The invention will now be explained in detail with reference to the accompanying drawings showing embodiments thereof. In the figures, like reference numerals designate like components, and overlapping explanations are avoided.

Fig. 3 shows one-column portion of a memory cell array of a DRAM according to a first embodiment of the invention. This memory cell array consists of a plurality of cascade gate type memory cells as shown in Fig. 1, only two of which are shown as memory cells MC0 and MC1, for simplifying the explanation of the array. Reference symbols BL, $\overline{BL}$ designate complementary bit lines, reference symbols WL10 - WL40 and WL11 - WL41 word lines to be driven by a word line driving circuit (not shown), reference symbol SA a bit line sense amplifier (e.g. a latch type amplifier) for sensing the potentials of the bit lines, reference symbol REG a register for temporarily registering bit data read from a selected memory cell in a time series manner, reference symbol PR a bit line precharging circuit to be driven by a bit line precharging signal ϕ PR, reference symbol VPR a bit line precharging source, reference symbol CS a column selecting switch to be controlled by an output CD generated from a column decoder circuit (not shown), and reference symbols $\overline{I/O}$, I/O complementary input/output lines.

The above-described memory cells MCi (i = 0, 1, ...) each comprise a cascade gate having a plurality of MOS transistors, four transistors Q1 - Q4 in this embodiment, which are connected by cascade connection, and a plurality of capacitors C1 - C4 (corresponding in number to the transistors Q1 - Q4) for storing a plurality of data, connected to those ends of the transistors which are located remote from a node N1, respectively. That end of the cascade gate which is located close to the node N1 is connected to the bit line BL. The capacitors C1 - C4 have the other ends connected to a capacitor common line. In this embodiment, one common plate electrode is provided for the capacitors C1 - C4, to supply them with a predetermined capacitor plate potential VPL.

The transistors Q1 - Q4 of the memory cell MC0 have their gates connected to the word lines WL10 - WL40, respectively. The word lines WL10 - WL40 are also connected to the gates of transistors Q1 - Q4 of each of memory cells (not shown) arranged in the same row as the memory cell MC0. Similarly, the transistors Q1 - Q4 of the memory cell MC1 have their gates connected to the word lines WL11 - WL41, respectively. The word lines WL11 - WL41 are also connected to the gates of transistors Q1 - Q4 of each of memory cells (not shown) arranged in the same row as the memory cell MC1.

The register REG has register elements of a number equal to or smaller by 1 than the capacitor number (= bit number) of the memory cell MCi.

Figs. 4, 5, and 6 show cases where the number of the elements of the register REG is smaller by 1 than that of the capacitors of the memory cell MCi, i.e., the number of the elements is three.

Referring to Fig. 4, reference symbols REG1 - REG3 denote first - third elements each consisting of a dynamic memory cell 41 having a transistor and a capacitor, respectively. Transistors TR1 - TR3 of the elements have ends connected to the bit line BL (or $\overline{BL}$), and gates connected to control signal lines RL1 - RL3, respectively. Capacitors RC1 - RC3 of the elements are connected to e.g. the same capacitor plate having a potential VPL.

The register shown in Fig. 5 differs from the register shown in Fig. 4 in that for example, the transistors TR1 and TR3 of the first and third elements REG 1 and REG 3 have ends connected to the bit line BL (or $\overline{BL}$), and the transistor TR2 of the remaining or second element REG2 has an end connected to the other bit line $\overline{BL}$ (or BL).

Referring to the register shown in Fig. 6, the elements REG1 - REG3 are each connected to both the bit lines BL and $\overline{BL}$, and also to the control signal lines RL1 - RL3, respectively.

Figs. 7 and 8 illustrates examples of the register elements REG1 - REG3 in Fig. 6.

The register element of Fig. 7 comprises a static memory cell (SRAM) 71 having a flip-flop circuit having a resistor R and two transfer gates. In this case, a P-channel MOS transistor may be used in place of the resistor R.

The register element of Fig. 8 comprises a dynamic memory cell 81 having two transistors and a capacitor connected between the transistors. This type memory cell is disclosed in "A Novel Memory Cell Architecture for High-Density DRAMs" by Y. Ohta, et al., 1989 Symposium on VLSI Circuits, Digest of Technical Papers, pp. 101-102, May 1989.

Fig. 9 is a waveform timing chart showing the operations of the sense amplifier SA, register REG, and word lines WL1 - WL4, which are connected to one memory cell MCi, in the case of using three register elements for the register in Fig. 3.

As is shown in Fig. 9, the word lines WL1 - WL4 are turned on in the order of WL1, WL2, WL3, and WL4, and off in the reverse order. Further, control signal lines RL1 - RL3 are turned on and off at points of time as shown, thereby operating the register elements in the order of first, second, and third, and then operating them in the reverse order. In the figure, point t1 denotes the time when the sense amplifier SA is operated, while point t2 denotes the time when the bit lines BL and $\overline{BL}$ are precharged to a predetermined potential (e.g. a half of the power source voltage).

By virtue of the above-described control, data items are successively read to the bit line BL from the capacitors C1, C2, C3, and C4 in the order mentioned, i.e., in the order from the capacitor closest to the bit line BL to that remotest therefrom. The data read out of the capacitors C1 - C3 are successively registered in the register REG. In this state, the read-out data or new data can be written into the capacitors C4, C3, C2, and C1 in the order mentioned, i.e., in the order of from the capacitor remotest from the bit line BL to that closest thereto.

Thus, 4-bit digital data stored in the capacitors C1 - C4 can be read out of the DRAM chip in a predetermined order, upon turning on the word lines WC1 - WC4 and operating the sense amplifier SA.

The above-described operation will be explained in more detail. When the word line WL1 is turned on after the bit lines BL and $\overline{BL}$ are precharged to the predetermined potential VPR by the bit line precharging circuit PR at the time point t1, the transistor Q1 is turned on, and the data in the capacitor C1 is read out through the transistor Q1. The read-out data is amplified by the sense amplifier SA. Then, the control signal line RL1 is turned on, and kept on until the amplified data is registered in the first element REG1 of the register REG. After the line RL1 is turned off, the bit lines BL and $\overline{BL}$ are precharged again at the time point t2. Then, the word line WL2 is turned on in a state in which the word line WL1 is on. At this time, the transistor Q2 is turned on, and the data stored in the capacitor C2 is read to the bit line BL through the transistors Q2 and Q1, where the sense amplifier SA is operated at the time point t1, thereby sensing the read-out data. Subsequently, the control signal line RL2 is turned on, and is kept on until the data read out of the capacitor C2 is amplified and then registered in the second element REG 2 of the register REG. In a similar way, the data stored in the capacitor C3 is registered in the third element REG 3 of the register REG. The bit lines BL and $\overline{BL}$ are again precharged at the time point t2, and the word line WL4 is turned on, thereby turning on the transistor Q4 and reading data from the capacitor C4 to the bit line BL through the transistors Q4 - Q1. The sense amplifier SA is operated at the time point t1, and senses the read-out data. Since at this time, the bit line BL is set at a rewriting potential corresponding to the data read out of the capacitor C4, rewriting is performed in the capacitor C4 upon turning off the word line WL4 and transistor Q4. Subsequently, the bit lines BL and $\overline{BL}$ are again precharged at the time point t2, then the control signal line RL3 is turned on, and the sense amplifier SA is operated at the time point t1. At this time, the bit lines BL and $\overline{BL}$ are set at a rewriting potential corresponding to the data registered in the third element REG3. When the word line WL3 is turned off in this state, the transistor Q3 is accordingly turned off, thereby performing rewriting in the capacitor C3. In a similar way, rewriting is performed successively in the capacitors C2 and C1.

Writing in the DRAM shown in Fig. 3 can be performed by setting data required for the bit lines BL and $\overline{BL}$, by means of a data-writing circuit (not shown) at the same time point as that of rewriting. Each column portion of the memory cell array is selectively connected to a data input/output circuit (not shown) by means of the input/output lines I/O and $\overline{I/O}$, to write input data, and to transfer read out data to the output side. The input/output lines I/O

and $\overline{I/O}$ each may be used as an input/output line, or may be used as a dedicated input or output line.

As is described above, since the DRAM of Fig. 3 employs a cascade gate type memory cell array, it can have a density much higher than the conventional DRAM employing one transistor/one capacitor type memory cell array, thereby remarkably reducing the cost of each bit. Thus, it is very advantageous to use the cascade gate type memory cell array of Fig. 3, so as to produce a large capacity DRAM, which is used in place of such a recording medium as a magnetic disk, at low cost by means of the conventional technique.

In this connection, it should be noted that each memory cell of the DRAM of Fig. 3 is accessed in a serial manner (i.e., data is serially written into or read out of each memory cell), so that its random accessibility is limited to some extent, and also the required access time is inevitably a little long. However, these disadvantages can be removed by performing serial-to-parallel or parallel-to-serial conversion of 4-bit data, thereby obtaining complete random accessibility as a DRAM capable of writing in and reading out data in units of 4 bits. Further, if the DRAM of Fig. 3 is modified to save power such that the memory cell array comprises a plurality of sub-arrays, and also that only some parts (e.g. two or four) of the sub-arrays are simultaneously activated, it can serve as a DRAM capable of writing in and reading out data in units of 8 or 16 bits by means of serial-to-parallel or parallel-to-serial conversion.

Moreover, to random access only the required data by using no serial-to-parallel conversion, it is not always needed to access all the capacitor of a memory cell, but it suffices if a capacitor storing the data required and a capacitor or capacitors (if exist) located closer to the node than the former are accessed. In this case, the access time varies in accordance with the distance between the node (bit line) and a capacitor selected. For dealing with this, it is considered that (a) a maximum access time is determined as the access time, or alternatively that (b) a waiting signal is being generated until the read-out data is output from the DRAM.

Further, it should be noted that some conventional DRAMs have a 4-bit serial access function such as a nibble mode, and that there have been rapidly increased applications such as block transfer between a cache memory and a DRAM or image data processing and storage, to which a serial access method can be applied. Accordingly, the DRAM of the invention may keep a serial access function since a slight limitation to its random accessibility does not so adversely act upon the actual operation. Thus, the DRAM of the invention can be estimated in spite of its serial access function by virtue of the above-described advantage that it can have high density.

In addition, although each register element is turned off at the time point shown in Fig. 9 after it is turned on again by a signal supplied through the corresponding control signal line RL1 - RL3, thereby terminating the writing, it may be turned off after the bit lines are precharged. However, in a case where accurate data need be kept registered in the register even after it is stored in the memory cell, it is desirable that the register is turned off at the timing shown in Fig. 9. Referring more strictly, the first turn-on of the register element is not necessarily performed at the time point shown in Fig. 9, after registering data read out of the capacitor, but the element may be turned on earlier than the timing shown in Fig. 9, if the data is assuredly registered therein.

Moreover, by setting such that the remoter from the read-out node the capacitors C1 - C4 of the memory cell MCi are located, the larger capacitance they have, that gradual reduction in the voltage variation of the read-out/write-in node which occurs while the capacitors are successively accessed will be compensated, so that the voltage variation of the node will have substantially the same value when any of the capacitors is accessed, thereby preventing data from being erroneously read out.

If the register REG in Fig. 3 comprises four (equal to the number of the capacitors of the memory cell MCi) register elements, data items stored in the four capacitors are to be registered in the four register elements, respectively.

Fig. 10 shows one-column portion of the memory cell array of a DRAM according to a second embodiment of the invention. This memory cell array consists of a plurality of cascade gate type memory cells as shown in Fig. 2.

Each memory cell MCi (i = 0, 1, ...) in Fig. 10 consists of a cascade gate having (more than three) MOS transistors Q1 - Q5 connected to one another by cascade connection and connected between first and second nodes N1 and N2, and capacitors C1 - C4 for storing data each connected to a corresponding connecting node connecting adjacent two transistors. The first and second read-out/write-in nodes N1 and N2 are connected to one bit line BL. The transistors Q1 - Q5 of the memory cell MC0 have gates connected to word lines WL10 - WL50, respectively. The word lines WL10 - WL50 are also connected to corresponding transistors Q1 - Q5 of each of memory cells (not shown) arranged in the same row as the memory cell MC0. Similarly, the transistors Q1 - Q5 of the memory cell MC1 have gates connected to word lines WL11 - WL51, respectively, and the word lines WL11 - WL51 are also connected to corresponding transistors Q1 - Q5 of each of memory cells (not shown)

arranged in the same row as the memory cell MC1.

The register REG shown in Fig. 10 has four (equal to the number of the capacitors of the memory cell MCi) register elements REG1 - REG4, which have gates connected to control signal lines RL1 - RL4, respectively.

Fig. 11 is a waveform timing chart showing the operations of the sense amplifier SA, register REG, and word lines WL1 - WL5, which are connected to each memory cell MCi in Fig. 10. In the figure, time points t1 and t2 correspond to those shown in Fig. 9. As is evident from Fig. 11, the DRAM of Fig. 10 operates in a way similar to the DRAM of Fig. 3, and therefore its operation is not explained in detail. Thus, it is possible to successively read data items to the bit line BL from the capacitors C1 - C4 in the order mentioned, also at the same time to successively and temporarily store them in the register REG, and thereafter to successively write the data from the bit line BL to the capacitors C1 - C4 in the order mentioned. If the transistors Q1 - Q5 and register elements REG1 - REG4 are turned on and off in the order reverse to the first-mentioned case, it is possible to successively read data items to the bit line BL from the capacitors C4 - C1 in the order mentioned, i.e., in the order from the capacitor closest to the second node N2 to that furthest therefrom, also at the same time to successively and temporarily store them in the register REG, and thereafter to successively write the data from the bit line BL to the capacitors C4 - C1 in the order mentioned, i.e., in the order from the capacitor closest to the second node N2.

In the above-described embodiments, a complex memory including a cache memory can be employed by making the register REG consist of four SRAM cells serving as the cache memory. In this case, the cache memory greatly compensates the disadvantage of the memory cells MCi that they are serially accessed.

Fig. 12 shows another example of the register REG, in which the transistors Q1 - Q3 are connected to capacitors C1 - C3 in a manner similar to the memory cell shown in Fig. 1, and the gates of the transistors Q1 - Q3 are connected to control signal lines RL3 - RL1, respectively.

Fig. 13 illustrates a further example of the register REG, in which the transistors Q1 - Q4 are connected to capacitors C1 - C3 in a manner similar to the memory cell shown in Fig. 2, and the gates of the transistors Q1 - Q4 are connected to control signal lines RL1 - RL4, respectively.

Fig. 14 illustrates the operation of a DRAM according to a third embodiment of the invention in which the memory cell shown in Fig. 1 and the register shown in Fig. 12 are incorporated. In Fig. 14, time points t1 and t2 correspond to those shown in Fig. 9.

In the embodiments in which the sense amplifier SA is operated at the time point t1, if charging and discharging occur in the bit lines BL and $\overline{BL}$ during operation of the sense amplifier SA, the potential of the bit lines varies between the highest and lowest values of the power source at least seven times during reading data out of each memory cell MC, thereby increasing power consumption. A DRAM which can operate with small power consumption is shown in Fig. 15.

Fig. 15 illustrates a part of one-column portion of the memory cell array of a DRAM according to a fourth embodiment. In the DRAM, a pair of transfer gates (MOS transistors) TG are connected between the sense amplifier SA and bit lines BL and $\overline{BL}$. Reference symbols DL and $\overline{DL}$ denote digit lines which are parts of the bit lines, respectively. To successively read data items from the capacitors of a selected memory cell MCi, and then to store them, the transfer gates TG are operated as follows:

After the data items are transmitted from the capacitors to the sense amplifier SA, the transfer gates TG are turned off, thereby operating the sense amplifier SA. To rewrite (or write) data, the transfer gates TG are turned on, thereby making the sense amplifier SA charge and discharge the bit lines BL and $\overline{BL}$. Thus, the transfer gates are charged and discharged only at the time of rewriting (or writing), i.e., totally only four times, which reduces the power consumption.

Any of the above-described embodiments may be modified such that a differential type amplifier which compares the potential of the bit line with a reference potential is used as the sense amplifier SA, thereby setting the rewriting potential of the bit line by a data writing circuit (not shown) in accordance with the output of the amplifier.

The DRAMs of the invention can incorporate not only cascade gate type memory cells, but also semiconductor memory cells proposed by the inventor of the invention in USA application No. 6 8 7, 6 8 7.

Specifically, the capacitors C1 - C4 of the cascade gate type memory cell MCi each may have the other end supplied with an external power voltage Vcc or an external ground voltage Vss.

Further, a memory cell, to which a technique of operating its capacitor plate in synchronism with a clock signal is applied, may be used in place of the above-described memory cell MCi. This technique is disclosed in IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-17, NO. 5, p. 872 OCT. 1982, "A Storage-Node-Boosted RAM with Word-Line Delay Compensation" by K. Fujishima et al.

Alternatively, a memory cell, to which a technique of connecting a transfer gate to the both opposite ends of each capacitor is applied, may be

used in place of the memory cell MCi. This technique cell is disclosed in "A Novel Memory Cell Architecture for High-Density DRAMs" (Fig. 1b) by Y. Ohta, et al., 1989 Symposium of VLSI Circuits, Digest of Technical Papers, pp. 101-102.

Although the above-described embodiments are constructed such that the register REG temporarily stores the data read out of the memory cell MCi in a time series manner, there may alternatively be provided bit line sense amplifiers of a number equal to the number of the capacitors of each memory cell, which amplifiers also serve as register means. An example of this case is illustrated in Fig. 16 as a fifth embodiment.

Fig. 16 shows part of one-column portion of the memory array of a DRAM according to the fifth embodiment. As is shown in the figure, a pair of transfer gates TG are connected between each of sense amplifiers SA1 - SA4 and the bit lines BL and $\overline{BL}$, respectively, and are turned on and off by signals supplied through control signal lines ϕ 1 - ϕ 4.

Fig. 17 is a waveform timing chart showing the operations of the sense amplifiers SA1 - SA4, and word lines WL1 - WL4, which are connected to one memory cell MCi, in the case of using a cascade gate type memory cell as shown in Fig. 1, as the memory cell MC of the DRAM of Fig. 16. Time points t1 and t2 in the figure correspond to those shown in Fig. 9.

When the control signal line ϕ 1 is turned on, and the word line WL1 is turned on in a state where the bit lines BL and $\overline{BL}$ and sense amplifier SA1 are precharged, the data stored in the capacitor C1 of the memory cell MCi is transmitted to the sense amplifier SA1. Then, the control signal line ϕ 1 is turned off, and then the sense amplifier SA1 is operated, thereby amplifying and latching the data read out of the capacitor C1. Rewriting (or writing) is performed by precharging the bit lines BL and $\overline{BL}$, then selecting a sense amplifier, further charging or discharging the bit lines to a predetermined potential, and turning off a corresponding word line. If the sense amplifiers SA1 - SA4 consisting of CMOS transistors are used, and also if the potential of the bit lines can be set to the power source potential Vcc and to the ground potential Vss, the pre-charging of the bit lines can be omitted at the time of rewriting or writing. Further, the sense amplifiers SA1 - SA4 can serve as a cache memory by using them like a SRAM cell.

Fig. 18 shows part of one-column portion of the memory array of a DRAM according to a sixth embodiment. As is shown in the figure, the DRAM employs register elements REGi (i = 1, 2, 3, and 4) each consisting of a SRAM, also transfer gates TG to be controlled by signals supplied through control signal lines RLi (i = 1, 2, 3, and 4), two of which transfer gates are connected between each register element REGi and digit lines DL and $\overline{DL}$, respectively, and transfer gates TG2 to be controlled by signals supplied through column selection lines CSL, two of which transfer gates are connected between each register element REGi and input/output lines (I/O)i and $(\overline{I/O})$i, respectively. 4-bit data items are read at a time from one-column portion of the memory array of the DRAM.

Fig. 19 shows one register element REGi in the case of replacing the SRAM cell with a sense amplifier SAi.

In the above embodiments, the memory cell array has a folded bit line structure, it may have an open bit line structure.

Moreover, the invention may employ a so-called single end type sense amplifier having an input node connected to one bit line BL directly or by means of a transfer gate, etc, as is shown in Figs. 20 - 24.

Fig. 20 illustrates a circuit obtained by modifying the circuit of Fig. 3 such that the sense amplifier employed therein is replaced with a single end type sense amplifier.

Fig. 21 illustrates a circuit obtained by modifying the circuit of Fig. 10 such that the sense amplifier employed therein is replaced with a single end type sense amplifier.

Fig. 22 illustrates a circuit obtained by modifying the circuit of Fig. 15 such that the sense amplifier employed therein is replaced with a single end type sense amplifier. In this case, a transfer gate TG1' connected to one digit line $\overline{DL}$ may be removed since it is additionally provided only for preventing the circuit from being adversely affected by the transfer gate TG1 connected between the bit line BL and sense amplifier SA. Alternatively, the circuit may be modified such that a reference potential Vref is supplied to the sense amplifier through the transfer gate TG1'.

Fig. 23 illustrates a circuit obtained by modifying the circuit of Fig. 16 such that the sense amplifier employed therein is replaced with a single end type sense amplifier.

Fig. 24 illustrates a circuit obtained by modifying the circuit of Fig. 19 such that the sense amplifier employed therein is replaced with a single end type sense amplifier. Here, a transfer gate TG' is similar to that shown in Fig. 22.

In addition, to connect the transfer gate between the bit line and sense amplifier, it is possible to employ a so-called shared sense amplifier technique. Specifically, in a case where a single type sense amplifier is used as the sense amplifier in the circuit, and the shared sense amplifier technique is applied thereto, the circuit may be constructed such that a plurality of bit lines and transfer gates are connected to one sense amplifier, and

that one of the bit lines is selected by controlling the transfer gates to be connected to the sense amplifier. Further, in a case where a cell array of a folded bit line structure or open bit line structure is incorporated in the circuit, and the shared sense amplifier technique is applied thereto, the circuit may be constructed such that a plurality of pairs of bit lines and transfer gates are connected to one sense amplifier, and that one pair of the bit lines is selected by controlling the transfer gates to be connected to the sense amplifier.

The invention is not limited to the above-described embodiments, but may be modified without departing from the spirit and scope thereof.

Claims

1. A semiconductor memory device comprising:

   a memory cell array having a plurality of dynamic memory cells (MCi), each of the memory cells including a plurality of MOS transistors (Q1 - Q4) connected by cascade connection, capacitors (C1 - C4) for storing data each having an end connected to an end of a corresponding one of the MOS transistors; and

   register means arranged in the column portion of the memory cell array, for temporarily registering the data read from the memory cells in a time series manner.

2. The semiconductor memory device according to claim 1, characterized in that the register means is a register (REG) having register elements (REG1 - REG3) of a number smaller by one than the number of the capacitors of each of the memory cells.

3. The semiconductor memory device according to claim 2, characterized in that the register elements (REG1 - REG3) each comprise a dynamic memory cell (41) having one transistor and one capacitor.

4. The semiconductor memory device according to claim 2, characterized in that the register elements (REG1 - REG3) each comprise a static memory cell (71).

5. The semiconductor memory device according to claim 2, characterized in that the register elements (REG1 - REG3) each comprise a dynamic memory cell (81) having two transistors and one capacitor connected between the transistors.

6. The semiconductor memory device according to claim 1, characterized in that the register means is a register (REG) having register elements (REG1 - REG4) of a number equal to the number of the capacitors of each of the memory cells.

7. The semiconductor memory device according to claim 6, characterized in that the register elements (REG1 - REG4) each comprise a dynamic memory cell (41) having one transistor and one capacitor.

8. The semiconductor memory device according to claim 6, characterized in that the register elements (REG1 - REG4) each comprise a static memory cell (71).

9. The semiconductor memory device according to claim 6, characterized in that the register elements (REG1 - REG4) each comprise a dynamic memory cell (81) having two transistors and one capacitor connected between the transistors.

10. The semiconductor memory device according to claim 1, characterized in that the register means consists of a register (REG) having a plurality of MOS transistors (Q1 - Q3) connected by cascade connection and capacitors (C1 - C3) for storing data each having an end connected to an end of a corresponding one of the MOS transistors.

11. The semiconductor memory device according to claim 1, characterized in that the register means consists of sense amplifiers (SA1 - SA4) of a number equal to the number of the capacitors of each (MCi) of the memory cells (MC), the sense amplifiers controlling read-out/write-in of the data stored in the capacitors (C1 - C4) of the memory cells, and also temporarily registering the data.

12. The semiconductor memory device according to any one of claims 1 - 11, characterized by further comprising a first transfer gate (TG) connected between a bit line (BL) and a bit line sense amplifier (SA), the first transfer gate being turned on and off at predetermined time points.

13. The semiconductor memory device according to claim 8, characterized by further comprising a first transfer gate (TG) connected between a bit line (DL or $\overline{DL}$) and each of the register elements (REG1 - REG4) each consisting of a static memory cell, and to be controlled by a signal supplied through a corresponding control signal line (RL1 - RL4), and a second

transfer gate (TG2) connected between each of the register elements and an input/output line (I/O or $\overline{I/O}$), and to be controlled by a signal supplied through a column selection line (CSL).

14. The semiconductor memory device according to claim 11, characterized by further comprising a first transfer gate (TG) connected between a bit line (DL or $\overline{DL}$) and each of the register elements (REG1 - REG4) consisting of sense amplifiers (SA1 - SA4), respectively, and to be controlled by a signal supplied through a corresponding control signal line (RL1 - RL4), and a second transfer gate (TG2) connected between each of the register elements and an input/output line (I/O or $\overline{I/O}$), and to be controlled by a signal supplied through a column selection line (CSL).

15. The semiconductor memory device according to claim 13 or 14, characterized in that the second transfer gate (TG2) is controlled by a common column selection line (CSL), and data of a plurality of bits are read out at a time from a selected one of column portions of the memory cell array.

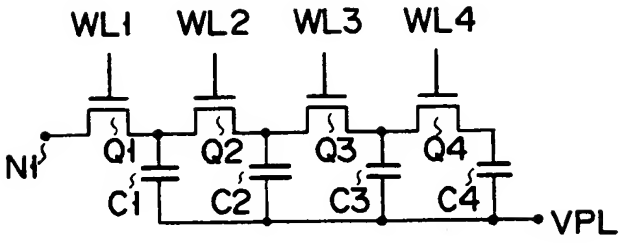


FIG. 1

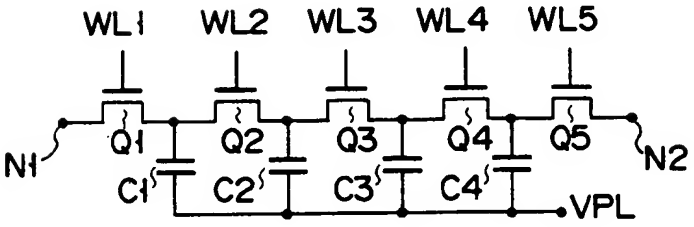


FIG. 2

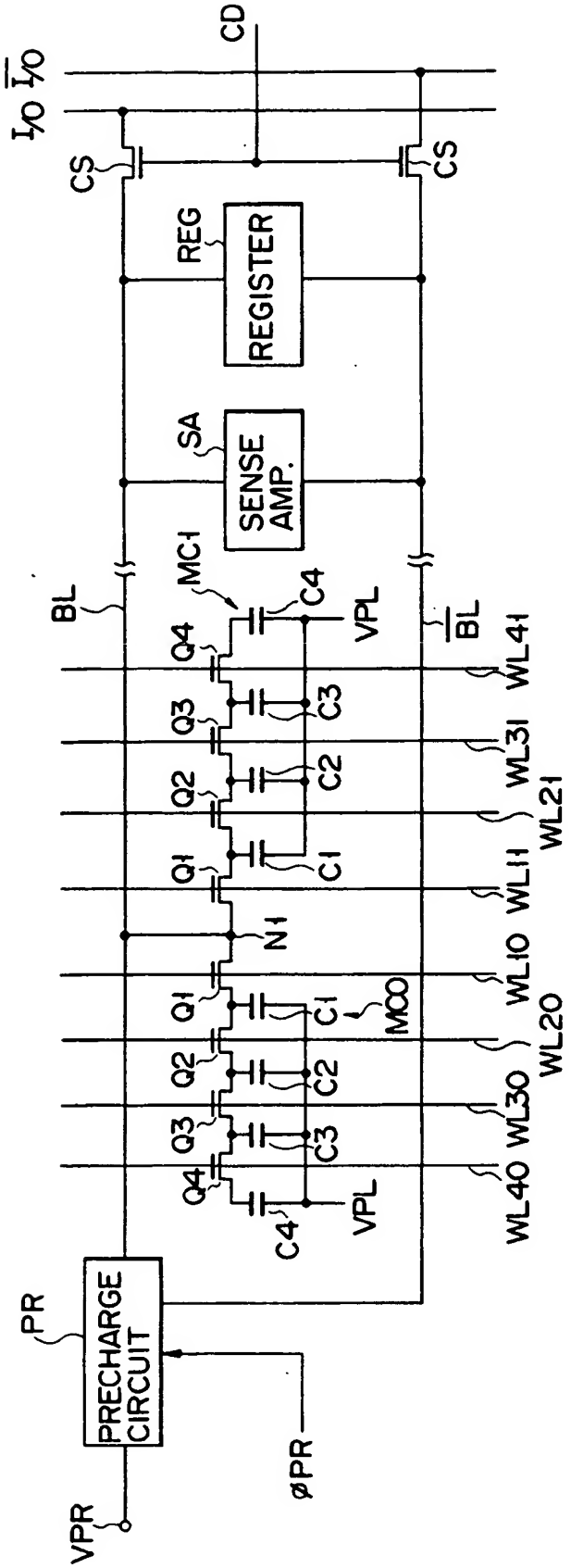


FIG. 3

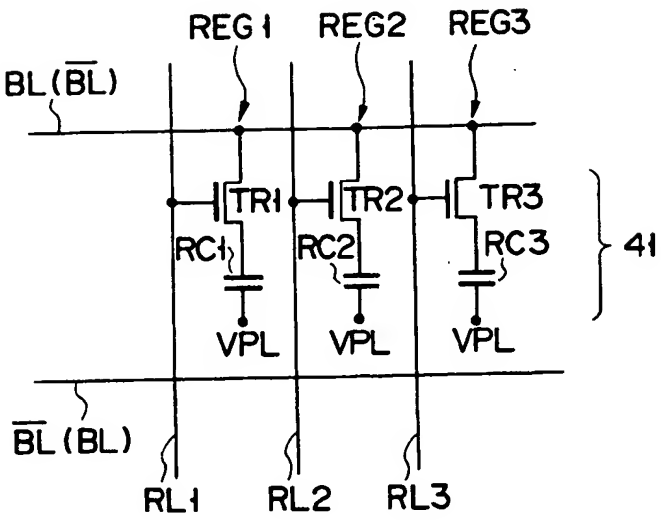


FIG. 4

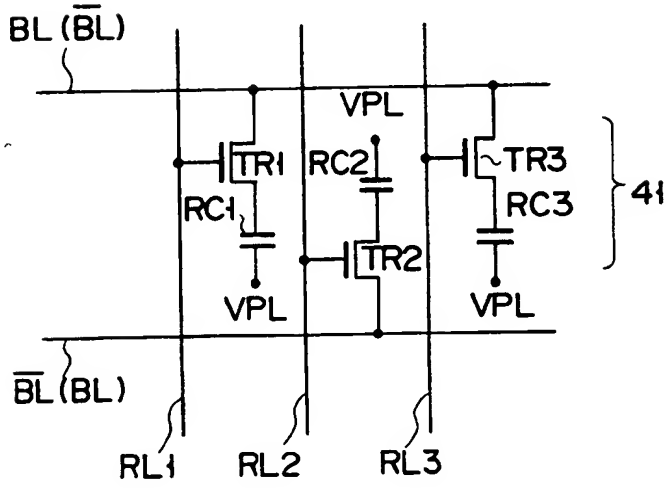


FIG. 5

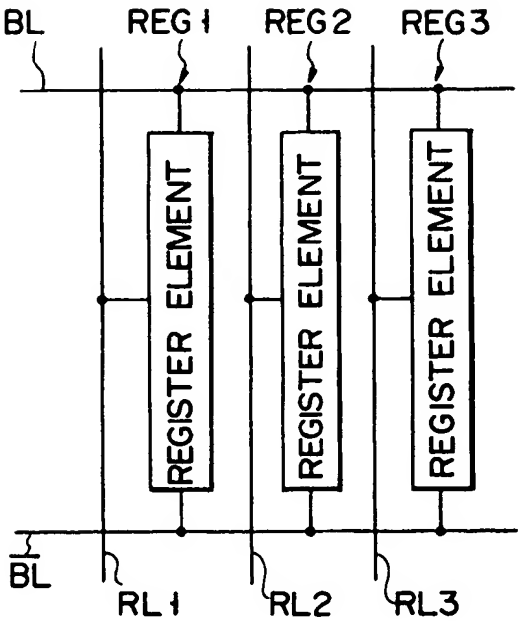


FIG. 6

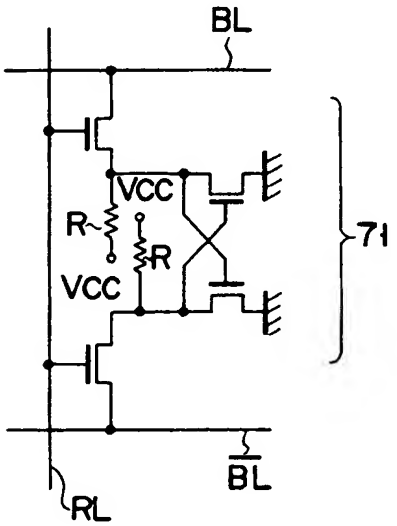


FIG. 7

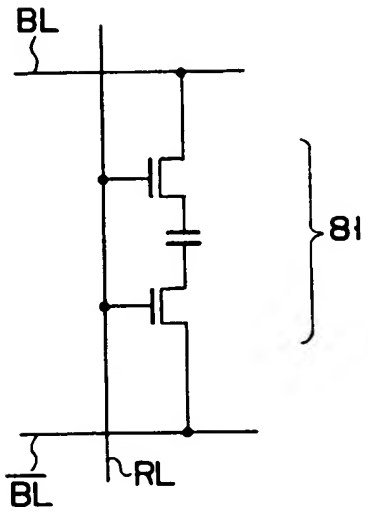


FIG. 8

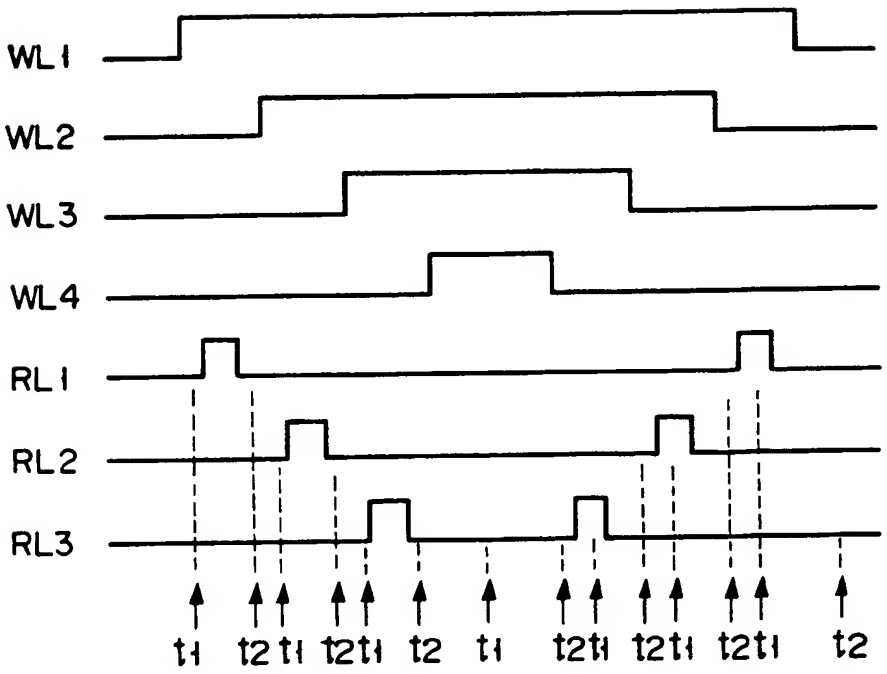


FIG. 9

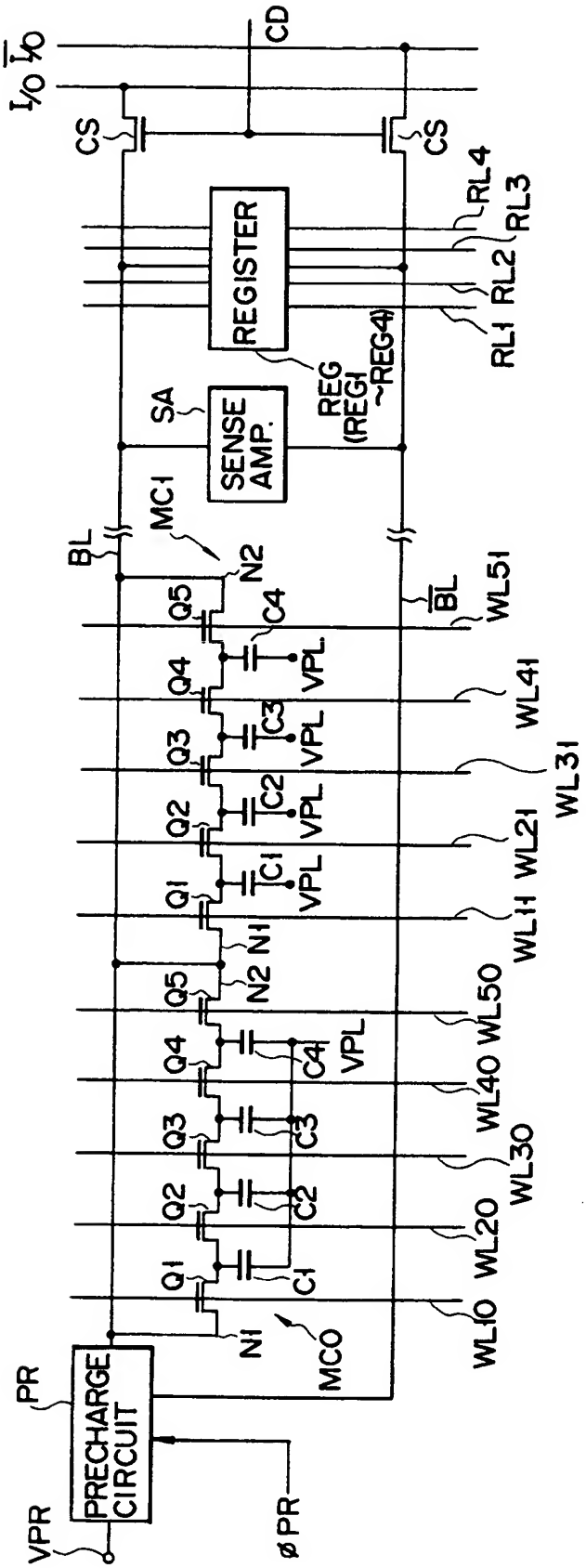


FIG. 10

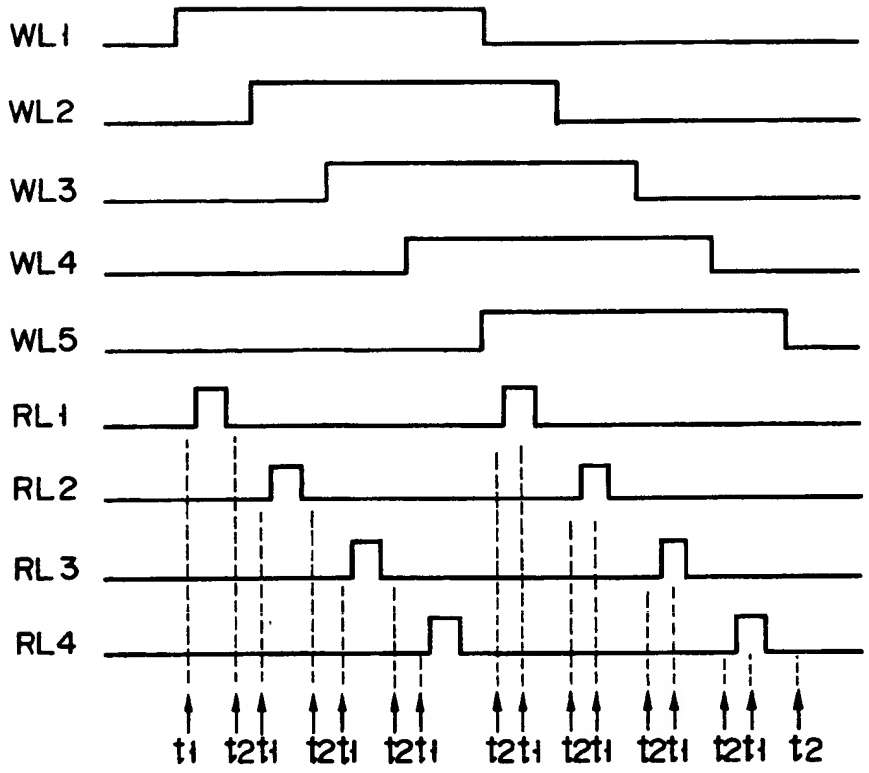


FIG. 11

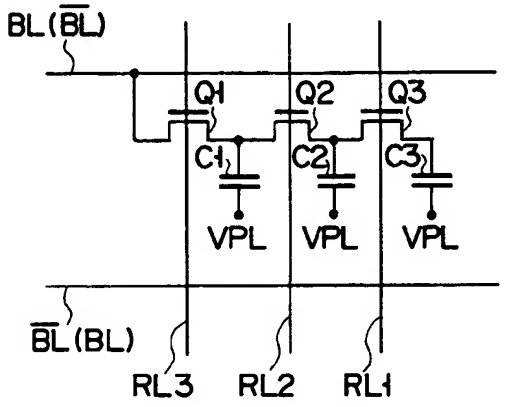


FIG. 12

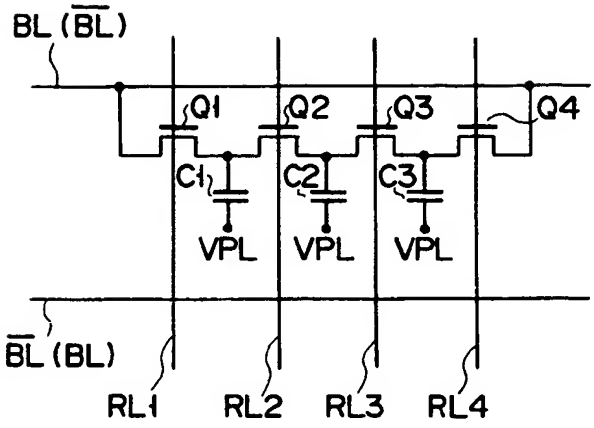


FIG. 13

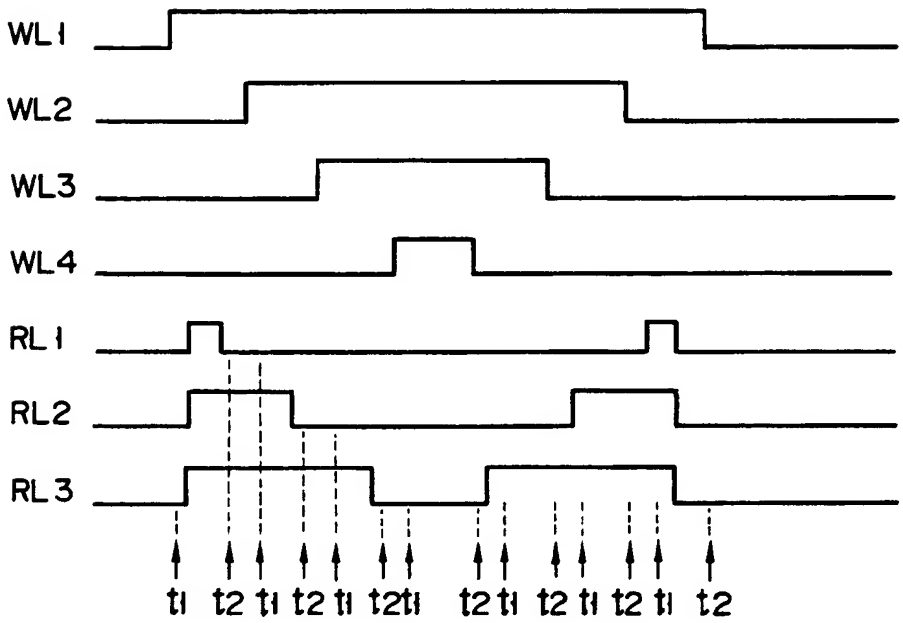


FIG. 14

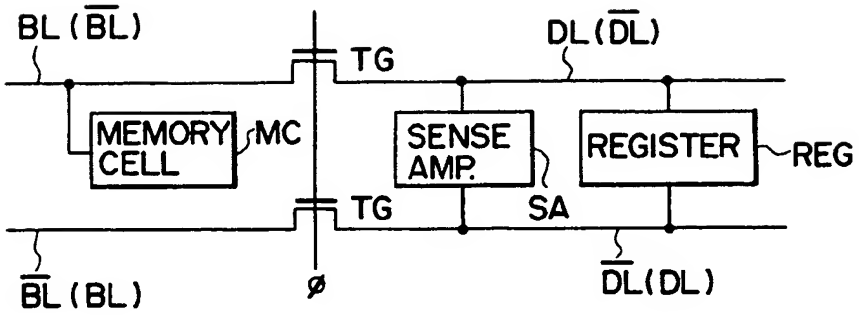


FIG. 15

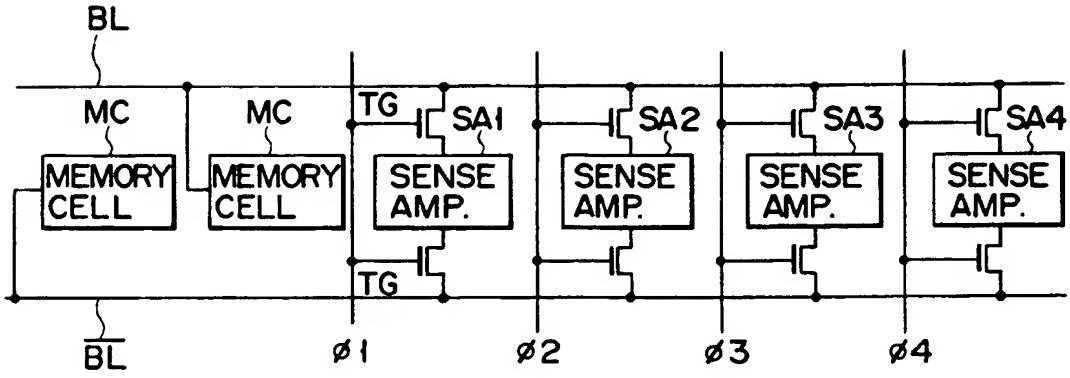
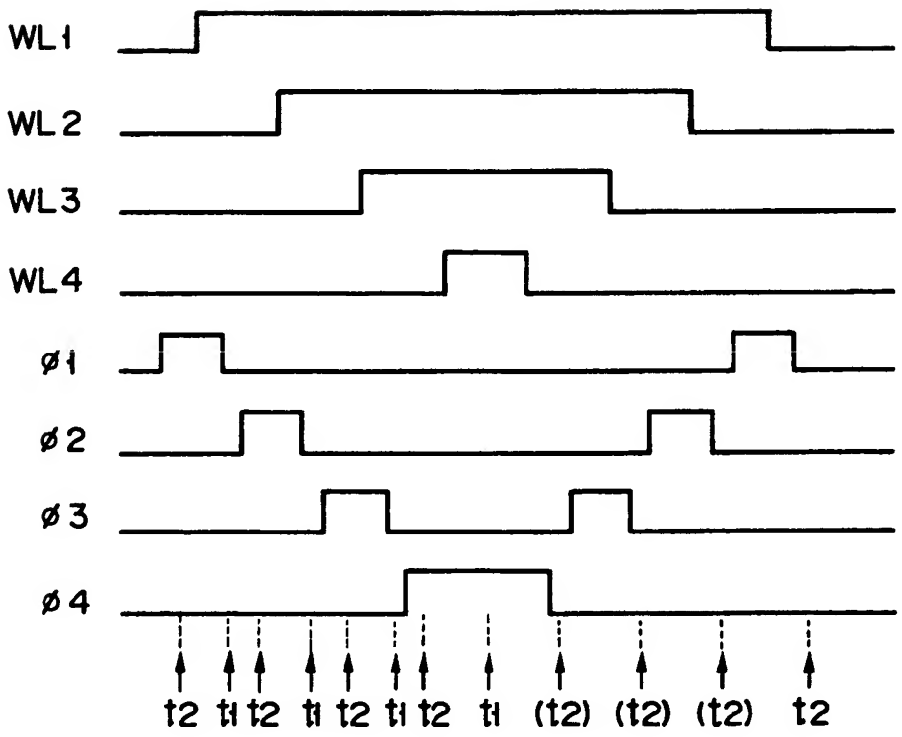


FIG. 16



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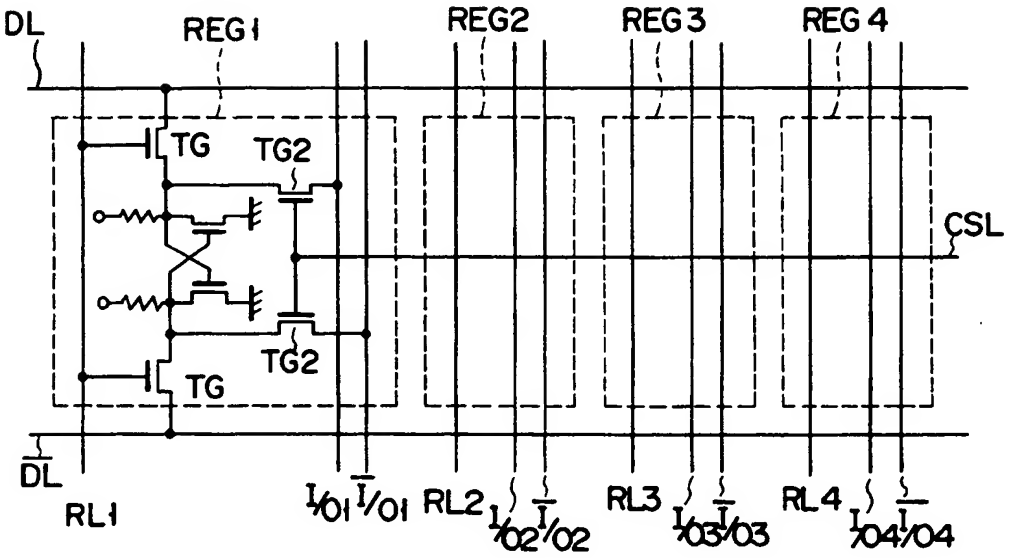

FIG. 18

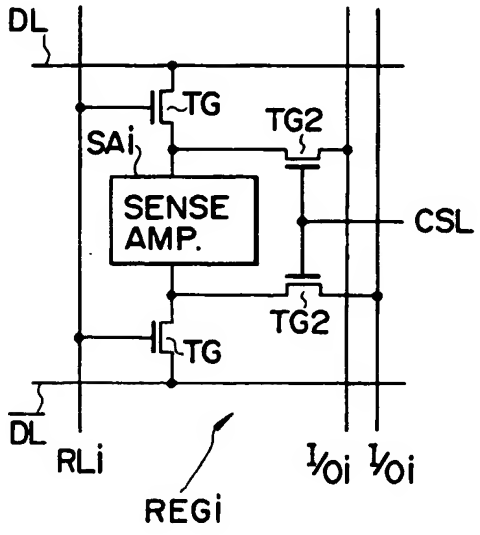

FIG. 19

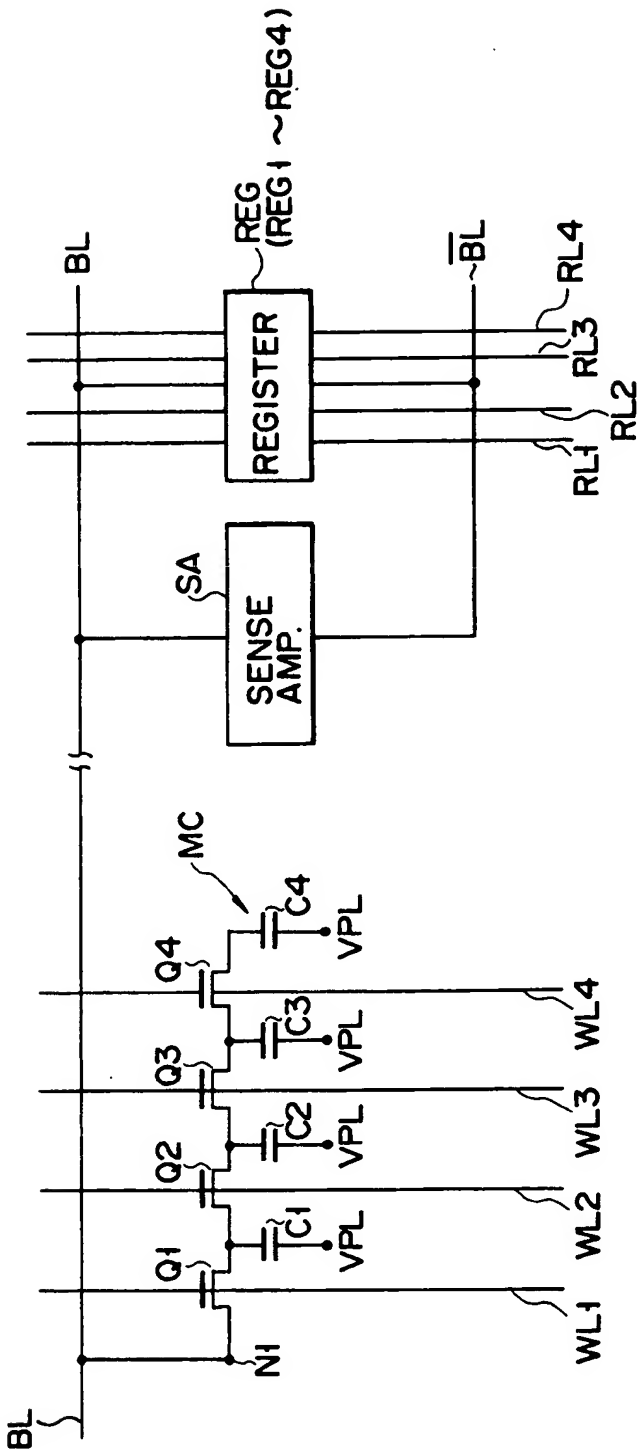

FIG. 20

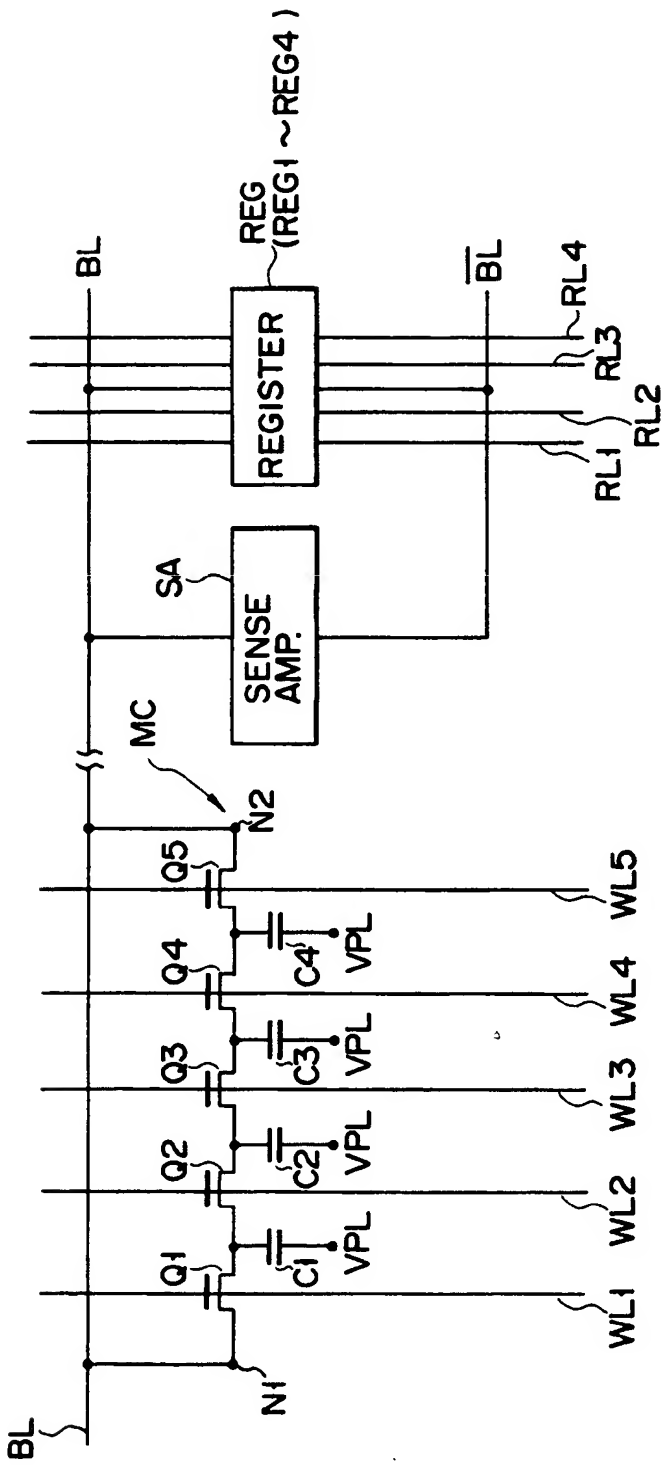

FIG. 21

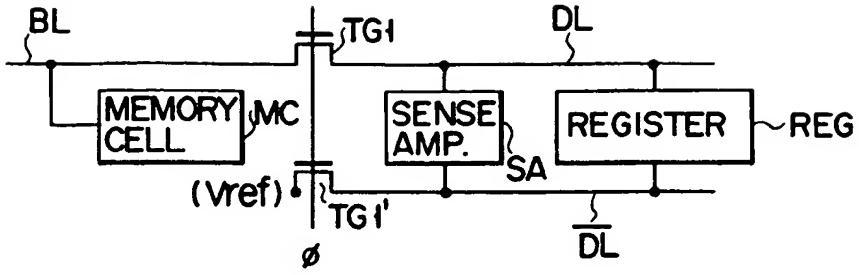

FIG. 22

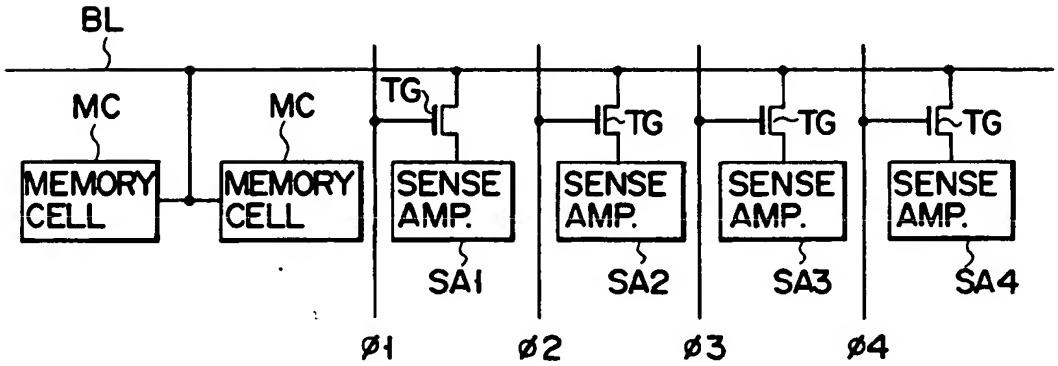

FIG. 23

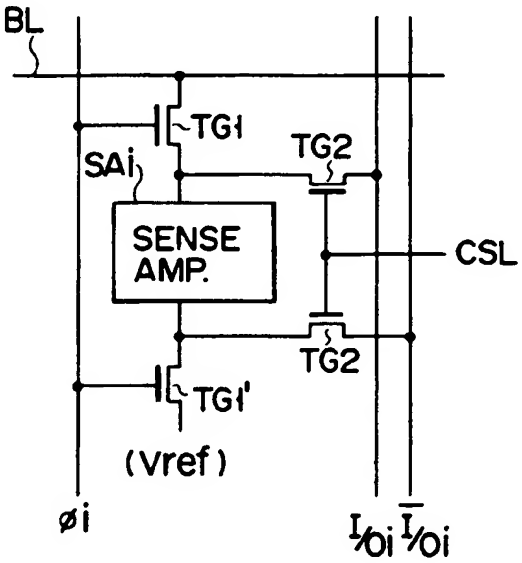

FIG. 24

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European Patent Office
Office européen des brevets

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13.02.91 JP 41316/91

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D-81904 München (DE)

(54) Semiconductor memory device.

(57) A semiconductor memory device comprising a memory cell array having a plurality of dynamic memory cells (MCi), each of the memory cells including a plurality of MOS transistors (Q1 - Q4) connected by cascade connection, capacitors (C1 - C4) for storing data each having an end connected to an end of a corresponding one of the MOS transistors, and a register arranged in a column portion of the memory cell array, for temporarily registering the data read from the memory cells in a time series manner.

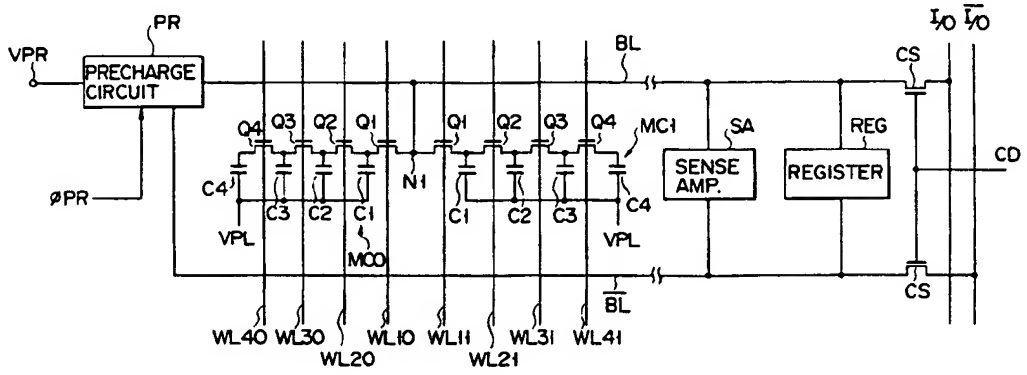

FIG. 3

Rank Xerox (UK) Business Services
(-/3.6/3.3.1)

BNSDOCID: <EP_____0463617A3_I_>

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 91 11 0563

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP-A-0 273 639 (TOSHIBA) * abstract * * column 4, line 26 - column 5, line 4; figures 3A,3B *	1-15	G11C11/56
A	SHARP TECHNICAL JOURNAL vol. 44, March 1990, JAPAN pages 47 - 50 OHTA ET AL. 'A NOVEL MEMORY CELL ARCHITECTURE FOR HIGH DENSITY DRAMS' * the whole document *	1-15	
A,D	1989 SYMPOSIUM ON VLSI CIRCUITS DIGEST OF TECHNICAL PAPERS May 1989, KYOTO JAPAN pages 101 - 102 OHTA ET AL. 'A NOVEL MEMORY CELL ARCHITECTURE FOR HIGH DENSITY DRAMS' * the whole document *	1-15	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			G11C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	11 JUNE 1993	STECCHINA A.

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